(57)   **ABSTRACT**

A memory controller with an integrated system management memory region is disclosed. The memory controller receives an SMI acknowledge signal from a processor. The processor then delivers a system management memory address to the memory controller. Instead of fetching SMI handler instructions from the address indicated by the processor, the memory controller instead fetches SMI handler instructions from its integrated system management memory region. At the end of the integrated system management memory's SMI handler, the processor is instructed to fetch instructions from the address originally specified by the processor. In this manner, a BIOS SMI routine may be executed after the integrated SMI routine is executed.